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Inventors:	Xavier S. Haurie, et al.
Patent No.:	6,917,321
Confirmation No:	1261
Issued:	July 12, 2005
For:	METHOD AND APPARATUS FOR USE IN SWITCHED CAPACITOR SYSTEMS
Examiner:	Phan, Trong Q.
Art Unit:	2818

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail, in an envelope addressed to: Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below.

Dated: September 8, 2006

Steven J. Henry

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REQUEST FOR ISSUANCE OF A CORRECTED PATENT UNDER 35 U.S.C. 254 AND 37 C.F.R 1.322(b) OR, IN THE ALTERNATIVE FOR A CERTIFICATE OF CORRECTION UNDER 37 C.F.R. 1.322(a)

Sir:

Pursuant to 35 U.S.C. §254 and 37 C.F.R. 1.322(b), Patentee requests issuance of a corrected patent. In the alternative, Patentee requests issuance of a Certificate of Correction to correct mistakes incurred through the fault of the Office, pursuant to 37 C.F.R. 1.322(a).

Upon inspection of the issued patent, Patentee has determined that the patent fails to contain a number of allowed claims from the Application and that it contains several claims that are not from this Application, at all, but from a companion application.

Attached hereto as Exhibit A is a document showing the chronological development of each amended claim in the application from its initial presentation through each amendment. The amended claims, coded in different shades of gray, correspond to their respective filing dates. Also, attached as Exhibit B hereto, is a chart that identifies the corresponding and non-corresponding patent and application claim numbers.

Exhibit B also identifies which claims of the published patent are not based in the '562 application.

It will be seen that of the 65 numbered claims in the patent, 37 or 38 are incorrect and should not be present, and that a similar number of allowed claims are missing.

Patentee has sought to understand how this could have occurred and has compared their file with the Imaged File Wrapper on PAIR. It was found that there is in PAIR an amendment, which, in fact, is not for this application, at all, but for a companion application serial number 09/575,561, attorney docket A0312/7408/SJH/MXS. We refer specifically to an amendment mailed November 30, 2001 and recorded in the IFW with a date of 12/31/2001. Accordingly, accompanying this document is a Petition to Expunge from the prosecution file of application serial number 09/575,562, that amendment from 09/575,561 erroneously entered into this file.

It is the recollection of the undersigned that Examiner Phan was aware of the Office's error in filing this amendment, which became known to Mr. Phan and the undersigned in connection with a telephone discussion regarding either this or one of the companion applications. In the course of that telephone conversation, it became clear that we were not looking at the same claims and that the clerical staff of the Office had misfiled an amendment. It was not known by the undersigned until now, however, that the misfiled amendment was still in the file. Mr. Phan and the undersigned had cleared up the claims in the '562 application and Mr. Phan was going to take steps to remove the '561 amendment from the file. Apparently that did not happen. Mr. Phan was not confused. He allowed the correct claims but the Publication Branch became confused by the erroneous inclusion in the prosecution history of an amendment that did not apply to this application, with rather disastrous impact on the claims printed in the patent.

Since approximately half the claims are in error, Patentee believes that both the assignee and the public would best be served by issuance of a corrected patent, instead of simply a Certificate of Correction. However, a Certificate of Correction form also is enclosed.

Respectfully submitted,

Xavier S. Haurie et al., Patentee

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Docket No.: A0312.70400US00
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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.	:	6917321
APPLICATION NO.	:	09/575562
ISSUE DATE	:	July 12, 2005
INVENTOR(S)	:	Xavier S. Haurie et al.

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims, replace claims 5 through 65 with the following list of claims:

5. The DAC of claim 1, wherein for each of the plurality of sub DACs, the associated capacitance comprises a single capacitor.

6. The DAC of claim 1, wherein at least a portion of the plurality of switched capacitor cells form a closed loop.

7. The DAC of claim 1, wherein the DAC comprises a plurality of switched capacitor cells used in forming the switched capacitor network, each of at least two of the plurality of switched capacitor cells has a orientation direction, and the at least two of the plurality of switched capacitor cells are oriented such that the orientation direction of at least one of the at least two of the plurality of switched capacitor cells is angularly offset relative to the orientation direction of at least one other of the at least two of the plurality of

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switched capacitor cells, the angular offset being substantially, ninety degrees.

8. The DAC of claim 1, wherein the DAC comprises a plurality of switched capacitor cells used in forming the switched capacitor network, each of at least four of the plurality of switched capacitor cells has a orientation direction, and the orientation direction of each one of the at least four of the plurality of switched capacitor cells is angularly offset relative to the orientation directions of the others of the at least four of the plurality of switched capacitor cells .

9. A DAC comprising:

a switched capacitor network that receives an equally-weighted multi-bit digital signal and outputs one or more analog signals, wherein at least one of the one or more analog signals comprises a single packet of charge indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

10. The DAC of claim 9, wherein the one or more analog signals comprises exactly one signal.

11. The DAC of claim 9, wherein the one or more analog signals comprises two or more analog signals, wherein at least two of the two or more analog signals comprises a single packet of charge indicative of a sum of equally weighted values of each bit in the multi-bit signal.

12. A DAC comprising:

a switched capacitor network that receives an equally-weighted multi-bit digital signal, the switched capacitor network having a plurality of sub DACs, at least two of the plurality of sub DACs sharing charge with one another, wherein the switched capacitor network outputs an analog signal

indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

13. The DAC of claim 12, wherein for each of the plurality of sub DACs, the associated capacitance comprises a single capacitor.

14. The DAC of claim 12, wherein at least a portion of the plurality of switched capacitor cells form a closed loop.

15. The DAC of claim 12, wherein the DAC comprises a plurality of switched capacitor cells used in forming the switched capacitor network, each of at least two of the plurality of switched capacitor cells has a orientation direction, and the at least two of the plurality of switched capacitor cells are oriented such that the orientation direction of at least one of the at least two of the plurality of switched capacitor cells is angularly offset relative to the orientation direction of at least one other of the at least two of the plurality of switched capacitor cells.

16. The DAC of claim 12, wherein the DAC comprises a plurality of switched capacitor cells used in forming the switched capacitor network, each of at least four of the plurality of switched capacitor cells has an orientation direction, and the orientation direction of each one of the at least four of the plurality of switched capacitor cells is angularly offset relative to the orientation directions of the others of the at least four of the plurality of switched capacitor cells.

17. A method of converting a multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal comprising:

charging each of a plurality of capacitors to a value corresponding to a value of a bit in the multi-bit signal, wherein the charge on each capacitor corresponds to a weight of the value of a corresponding bit;

temporarily connecting at least two of the plurality of capacitors to one another to share charge; and

providing at least one analog output signal indicative of a sum of values of each bit in the multi-bit signal, after disconnecting the at least two of the plurality of capacitors from one another.

18. The method of claim 17, wherein the method further comprises connecting each of the plurality of capacitors to at least one other of the plurality of capacitors.

19. The method of claim 17, wherein the method further comprises connecting all of the plurality of capacitors together so the value of each of the plurality of capacitors is substantially a same value.

20. The method of claim 19, wherein the charge on each of the plurality of capacitors is substantially a same charge.

21. A method of converting a equally-weighted multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal comprising:

charging each of a plurality of capacitors to a value corresponding to a value of a bit in the equally-weighted multi-bit signal, and

generating a single packet of charge on at least one capacitor indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

22. The method of claim 21, wherein the method further comprises connecting each of the plurality of capacitors to at least one other of the plurality of capacitors.

23. The method of claim 21, wherein the method further comprises charging each of the plurality of capacitors to a level indicative of a value of correspondence and connecting all of the plurality of capacitors together so each of the capacitors has a charge which is substantially a same charge.

24. A method of converting an equally weighted multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal comprising:

charging each of a plurality of capacitors to a value corresponding to a value of a bit in the equally-weighted multi-bit signal, and

connecting at least two of the plurality of capacitors to one another to share charge.

25. The method of claim 24, wherein the method further comprises connecting each of the plurality of capacitors to at least one other of the plurality of capacitors.

26. The method of claim 24, wherein the method further comprises charging each of the plurality of capacitors to a level indicative of a value of correspondence and connecting all of the plurality of capacitors together so each of the capacitors has a charge which is substantially a same charge.

27. A DAC comprising:

means for charging each of a plurality of capacitors to a value corresponding to a value of a bit in a multi-bit signal, wherein the charge on each capacitor corresponds to a weight of the value of a corresponding bit;

means for temporarily connecting at least two of the plurality of capacitors to one another to share charge; and

means for providing at least one analog output signal indicative of a sum of values of each bit in the multi-bit signal, after disconnecting the at least two of the plurality of capacitors from one another.

28. The DAC of claim 27, wherein the DAC further comprises means for connecting each of the plurality of capacitors to at least one other of the plurality of capacitors.

29. The DAC of claim 27, wherein the DAC further comprises means for connecting all of the capacitors together so each has substantially the same value.

30. The DAC of claim 29, wherein each of the capacitors has substantially the same charge.

31. A DAC comprising:

means for charging each of a plurality of capacitors to a value corresponding to a value of a bit in an equally-weighted multi-bit signal, and

means for generating a single packet of charge on at least one capacitor indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

32. The DAC of claim 31, further comprising means for connecting each of the plurality of capacitors to at least one other of the plurality of capacitors.

33. The DAC of claim 31 further comprising means for charging each of the plurality of capacitors to a level indicative of a value of correspondence and connecting all of the plurality of capacitors together so a charge of each of the capacitors is substantially a same charge.

34. A DAC comprising:

means for charging each of a plurality of capacitors to a value corresponding to a value of a bit in an equally-weighted multi-bit signal, and

means for connecting at least two of the plurality of capacitors to one another to share charge.

35. The DAC of claim 34, further comprising means for connecting each of the plurality of capacitors to at least one other of the plurality of capacitors.

36. The DAC of claim 34 further comprising means for charging each of the plurality of capacitors to a level indicative of a value of correspondence and connecting all of the plurality of capacitors together so a charge of each of the capacitors is substantially a same charge.

37. An integrated circuit comprising:

an integrated switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, the integrated switched capacitor network having a charge sharing operating state in which at least two of the plurality of sub DACs share charge with one another, and having an operating state, initiated subsequent to the charge sharing operating state, in which the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

38. An integrated circuit comprising:

an integrated switched capacitor network that receives an equally-weighted multi-bit digital signal and outputs one or more analog signals, wherein at least one of the one or more analog signals comprises a single packet of charge indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

39. An integrated circuit comprising:

an integrated switched capacitor network that receives an equally-weighted multi-bit digital signal, the switched capacitor network having a plurality of sub DACs, at least two of the plurality of sub DACs sharing charge with one another, wherein the switched capacitor network outputs an analog signal indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

40. The DAC of claim 1 wherein each of the plurality of sub DACs shares charge with at least one other of the plurality of sub DACs to generate at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

41. The DAC of claim 1 wherein the switched capacitor network generates the at least one analog signal in response to the charge received by the capacitance of each of the plurality of sub DACs in response to the associated bit.

42. The DAC of claim 12 wherein each of the plurality of sub DACs shares charge with at least one other of the plurality of sub DACs to generate at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

43. The DAC of claim 12 wherein the switched capacitor network generates the at least one analog signal in response to the charge received by the capacitance of each of the plurality of sub DACs in response to the associated bit.

44. The method of claim 17 further comprising generating at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal in response to the charge stored on each of the plurality of capacitors by the step of charging.

45. The method of claim 17 wherein connecting comprises connecting each of the plurality of sub DACs with at least one other of the plurality of sub DACs to share charge and generate at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal.

46. The method of claim 24 further comprising generating at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal in response to the charge stored on each of the plurality of capacitors by the step of charging.

47. The method of claim 24 wherein connecting comprises connecting each of the plurality of sub DACs with at least one other of the plurality of sub DACs to share charge and generate at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal.

48. The DAC of claim 27 further comprising means for generating at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal in response to the charge stored on each of the plurality of capacitors by the step of charging.

49. The DAC of claim 27 wherein means for connecting comprises means for connecting each of the plurality of sub DACs with at least one other of the plurality of sub DACs to share charge and generate at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal.

50. The DAC of claim 34 further comprising means for generating at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal in response to the charge stored on each of the plurality of capacitors by the step of charging.

51. The DAC of claim 34 wherein means for connecting comprises means for connecting each of the plurality of sub DACs with at least one other of the plurality of sub DACs to share charge and generate at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal.

52. The DAC of claim 37 wherein each of the plurality of sub DACs shares charge with at least one other of the plurality of sub DACs to generate at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

53. The DAC of claim 37 wherein the switched capacitor network generates the at least one analog signal in response to the charge received by the capacitance of each of the plurality of sub DACs in response to the associated bit.

54. The DAC of claim 39 wherein each of the plurality of sub DACs shares charge with at least one other of the plurality of sub DACs to generate at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

55. The DAC of claim 39 wherein the switched capacitor network generates the at least one analog signal in response to the charge received by the capacitance of each of the plurality of sub DACs in response to the associated bit.

56. The DAC of claim 1 wherein the DAC has more than one charge sharing operating state in which at least two of the plurality of sub DACs share charge with one another.

57. The DAC of claim 1 wherein the DAC has more than one operating state, subsequent to the charge sharing operating state, in which the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

58. A DAC comprising:
a switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, the DAC having an operating state in which at least two of the plurality of sub DACs share charge with one another, and having an operating state in which fewer than all of the plurality of sub DACs are connected to an output terminal and the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

59. The DAC of claim 58 wherein the DAC has more than one charge sharing operating state in which at least two of the plurality of sub DACs share charge with one another.

60. The DAC of claim 58 wherein the DAC has more than one operating state in which fewer than all of the plurality of sub DACs are connected to an output terminal and the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

61. The DAC of claim 58 wherein in the operating state in which fewer than all of the plurality of sub DACs are connected to an output terminal and the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal, the sub DACs that are connected to the output terminal deliver charge to said output terminal.

62. A method of converting a multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal comprising the steps of:

charging each of a plurality of capacitors to a value corresponding to a value of a bit in the multi-bit signal, wherein the charge on each capacitor corresponds to a weight of the value of a corresponding bit;

connecting at least two of the plurality of capacitors to one another to share charge; and

connecting fewer than all of the plurality of sub DACs to an output terminal to provide at least one analog output signal indicative of a sum of values of each bit in the multi-bit signal.

63. A DAC comprising:

means for charging each of a plurality of capacitors to a value corresponding to a value of a bit in a multi-bit signal, wherein the charge on each capacitor corresponds to a weight of the value of a corresponding bit;

means for connecting at least two of the plurality of capacitors to one another to share charge; and

means for connecting fewer than all of the plurality sub DACs to an output terminal to provide at least one analog output signal indicative of a sum of values of each bit in the multi-bit signal.

64. An integrated circuit comprising:

an integrated switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, the integrated switched capacitor network having an operating state in which at least two of the plurality of sub DACs share charge with one another, and having an operating state in which fewer than all of the plurality of sub DACs are connected to an output terminal and the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

65. The DAC of claim 15 wherein the angular offset is substantially ninety degrees.

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Dated: September 8 2006 Signature: ______________ (Steven J. Henry)

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2/13/03 = [illegible]

Exhibit A

Chronological Development of Each Claim in
U.S. Patent No. 6,917,321, Issued July 12, 2005

1. (Amended) A DAC comprising:

a switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, the DAC having a charge sharing operating state in which at least two of the plurality of sub DACs share ~~sharing~~ charge with one another, and having an operating state, initiated subsequent to the charge sharing operating state, in which the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

2. (Amended) The DAC of claim 1, wherein the multi-bit digital signal is an equally-weighted multi-bit digital signal, and the associated amount of charge is the same for each of the plurality of sub DACs~~,~~

3. (Amended) The DAC of claim 1, wherein the multi-bit digital signal is an equally-weighted multi-bit digital signal, and the associated capacitance is the same for each of the plurality of sub DACs.

4. (Original) The DAC of claim 1, wherein each of the plurality of sub DACs shares charge with one another, and the switched capacitor network outputs an analog signal indicative of a sum of values of each bit in the multi-bit signal.

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5. The DAC of claim 1, wherein ~~**there is a one to one relationship between a number of capacitors and a number of bits**~~ **for each of the plurality of sub DACs, the associated capacitance comprises a single capacitor**.

6. (Original) The DAC of claim 1, wherein at least a portion of the plurality of switched capacitor cells form a closed loop.

7. (Amended) The DAC of claim 1, wherein the DAC comprises a plurality of switched capacitor cells used in forming the switched capacitor network, each of at least two of the plurality of switched capacitor cells has a orientation direction, and the at least two of the plurality of switched capacitor cells are oriented such that the orientation direction of at least one of the at least two of the plurality of switched capacitor cells is angularly offset ~~rotate substantially ninety degrees~~ relative to the orientation direction of at least one other of the at least two of the plurality of switched capacitor cells, the angular offset being substantially ninety degrees.

8. (Amended) The DAC of claim 1, wherein the DAC comprises a plurality of switched capacitor cells used in forming the switched capacitor network, each of at least four of the plurality of switched capacitor cells has ~~have~~ a orientation direction, and the orientation direction of each one of the at least four of the plurality of switched capacitor cells ~~has an~~ is angularly offset relative to the orientation directions of the others of the at least four of the plurality of switched capacitor cells.

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9. (Amended) A DAC comprising:

a switched capacitor network that receives an equally-weighted multi-bit digital signal and outputs one or more analog signals, wherein at least one of the one or more analog signals comprises a single packet of charge indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

10. (Original) The DAC of claim 9, wherein the one or more analog signals comprises exactly one signal.

11. (Original) The DAC of claim 9, wherein the one or more analog signals comprises two or more analog signals, wherein at least two of the two or more analog signals comprises a single packet of charge indicative of a sum of equally weighted values of each bit in the multi-bit signal.

12. (Amended) A DAC comprising:

a switched capacitor network that receives an equally-weighted multi-bit digital signal, the switched capacitor network having a plurality of sub DACs, at least two of the plurality of sub DACs sharing charge with one another, wherein the switched capacitor network outputs an analog signal indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

13. (Amended) The DAC of claim 12, wherein ~~there is a one to one relationship between a number of capacitors and a number of bits~~ **for each of the plurality of sub DACs, the associated capacitance comprises a single capacitor.**

14. (Original) The DAC of claim 12, wherein at least a portion of the plurality of switched capacitor cells form a closed loop.

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15. (Amended) The DAC of claim 12, wherein the DAC comprises a plurality of switched capacitor cells used in forming the switched capacitor network, each of at least two of the plurality of switched capacitor cells has a orientation direction, and the at least two of the plurality of switched capacitor cells are oriented such that the orientation direction of at least one of the at least two of the plurality of switched capacitor cells is angularly offset ~~rotated substantially ninety degrees~~ relative to the orientation direction of at least one other of the at least two ~~one~~ of the plurality of switched capacitor cells.

16. (Amended) The DAC of claim 12, wherein the DAC comprises a plurality of switched capacitor cells used in forming the switched capacitor network, each of at least four of the plurality of switched capacitor cells has ~~have a~~ an orientation direction, and the orientation direction of each one of the at least four of the plurality of switched capacitor cells ~~has an~~ is angularly offset relative to the orientation directions of the others of the at least four of the plurality of switched capacitor cells.

17. (Amended) A method of converting a multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal comprising ~~the steps of~~:

charging each of a plurality of capacitors to a value corresponding to a value of a bit in the multi-bit signal, wherein the charge on each capacitor corresponds to a weight of the value of a corresponding bit; ~~and~~

temporarily connecting at least two of the plurality of capacitors to one another to share charge ~~with one another~~; and

providing at least one analog output signal indicative of a sum of values of each bit in the multi-bit signal, after disconnecting the at least two of the plurality of capacitors from one another.

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18. (Original) The method of claim 17, wherein the method further comprises connecting each of the plurality of capacitors to at least one other of the plurality of capacitors.

19. (Amended) The method of claim 17, wherein the method further comprises connecting all of the plurality of capacitors together so ~~each~~ the value of each of the plurality of capacitors ~~has~~ is substantially ~~the]~~ a same value.

20. (Amended) The method of claim 19, wherein ~~each of~~ the charge on each of the plurality of capacitors is substantially a same charge.

21. (Amended) A method of converting a equally-weighted multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal comprising ~~the steps of~~:

charging each of a plurality of capacitors to a value corresponding to a value of a bit in the equally-weighted multi-bit signal, and

generating a single packet of charge on at least one capacitor indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

22. (Original) The method of claim 21, wherein the method further comprises connecting each of the plurality of capacitors to at least one other of the plurality of capacitors.

23. (Amended) The method of claim 21, wherein the method further comprises charging each of the plurality of capacitors to a level indicative of a value of correspondence and connecting all of the plurality of capacitors together so each of the capacitors has a charge which is substantially a ~~has the~~ same charge.

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24. (Amended) A method of converting an equally weighted multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal comprising ~~the steps of~~:

charging each of a plurality of capacitors to a value corresponding to a value of a bit in the equally-weighted multi-bit signal , and

connecting at least two of the plurality of capacitors to one another to share charge ~~with one another~~.

25. (Original) The method of claim 24, wherein the method further comprises connecting each of the plurality of capacitors to at least one other of the plurality of capacitors.

26. (Amended) The method of claim 24, wherein the method further comprises charging each of the plurality of capacitors to a level indicative of a value of correspondence and connecting all of the plurality of capacitors together so each of the capacitors has a charge which is substantially a ~~has~~ same charge.

27. (Amended) A DAC comprising:

means for charging each of a plurality of capacitors to a value corresponding to a value of a bit in ~~the~~ a multi-bit signal, wherein the charge on each capacitor corresponds to a weight of the value of a corresponding bit; ~~and~~

means for temporarily connecting at least two of the plurality of capacitors to one another to share charge ~~with one another;~~ and

means for providing at least one analog output signal indicative of a sum of values of each bit in the multi-bit signal, after disconnecting the at least two of the plurality of capacitors from one another.

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28. (Original) The DAC of claim 27, wherein the DAC further comprises means for connecting each of the plurality of capacitors to at least one other of the plurality of capacitors.

29. (Original) The DAC of claim 27, wherein the DAC further comprises means for connecting all of the capacitors together so each has substantially the same value.

30. (Original) The DAC of claim 29, wherein each of the capacitors has substantially the same charge.

31. (Amended) A DAC comprising:

means for charging each of a plurality of capacitors to a value corresponding to a value of a bit in ~~the~~ an equally-weighted multi-bit signal, and

means for generating a single packet of charge on at least one capacitor indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

32. (Original) The DAC of claim 31, further comprising means for connecting each of the plurality of capacitors to at least one other of the plurality of capacitors.

33. (Amended) The DAC of claim 31 further comprising means for charging each of the plurality of capacitors to a level indicative of a value of correspondence and connecting all of the plurality of capacitors together so a charge of each of the capacitors is substantially a ~~has~~ same charge.

Amendments Filed are Coded as Follows:
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34. (Amended) A DAC comprising:

means for charging each of a plurality of capacitors to a value corresponding to a value of a bit in ~~the~~ an equally-weighted multi-bit signal, and

means for connecting at least two of the plurality of capacitors to one another to share charge ~~with one another~~.

35. (Original) The DAC of claim 34, further comprising means for connecting each of the plurality of capacitors to at least one other of the plurality of capacitors.

36. (Amended) The DAC of claim 34 further comprising means for charging each of the plurality of capacitors to a level indicative of a value of correspondence and connecting all of the plurality of capacitors together so a charge of each of the capacitors is substantially a ~~has~~ same charge.

37. (Amended) An integrated circuit comprising:

an integrated [a] switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, the ~~DAC~~ **integrated switched capacitor network** having a charge sharing operating state in which at least two of the plurality of sub DACs share ~~sharing~~ charge with one another, and having an operating state, initiated subsequent to the charge sharing operating state, in which the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

Amendments Filed are Coded as Follows:

1/14/02 =
8/15/02 = **bold text**
2/13/03 =

38. (Amended) An integrated circuit comprising:

an integrated switched capacitor network that receives an equally-weighted multi-bit digital signal and outputs one or more analog signals, wherein at least one of the one or more analog signals comprises a single packet of charge indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

39. (Amended) An integrated circuit comprising:

an integrated switched capacitor network that receives an equally-weighted multi-bit digital signal, the switched capacitor network having a plurality of sub DACs, at least two of the plurality of sub DACs sharing charge with one another, wherein the switched capacitor network outputs an analog signal indicative of a sum of equally-weighted values of each bit in the multi-bit signal.

40. (New) The DAC of claim 1 wherein each of the plurality of sub DACs shares charge with at least one other of the plurality of sub DACs to generate at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

41. (New) The DAC of claim 1 wherein the switched capacitor network generates the at least one analog signal in response to the charge received by the capacitance of each of the plurality of sub DACs in response to the associated bit.

42. (New) (New) The DAC of claim 12 wherein each of the plurality of sub DACs shares charge with at least one other of the plurality of sub DACs to generate at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

Amendments Filed are Coded as Follows:

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8/15/02 = **bold text**
2/13/03 =

43. (New) The DAC of claim 12 wherein the switched capacitor network generates the at least one analog signal in response to the charge received by the capacitance of each of the plurality of sub DACs in response to the associated bit.

44. (New) The method of claim 17 further comprising generating at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal in response to the charge stored on each of the plurality of capacitors by the step of charging.

45. (New) The method of claim 17 wherein connecting comprises connecting each of the plurality of sub DACs with at least one other of the plurality of sub DACs to share charge and generate at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal.

46. (New) The method of claim 24 further comprising generating at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal in response to the charge stored on each of the plurality of capacitors by the step of charging.

47. (New) The method of claim 24 wherein connecting comprises connecting each of the plurality of sub DACs with at least one other of the plurality of sub DACs to share charge and generate at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal.

48. (New) The DAC of claim 27 further comprising means for generating at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal in response to the charge stored on each of the plurality of capacitors by the step of charging.

Amendments Filed are Coded as Follows:

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8/15/02 = **bold text**

2/13/03 =

49. (New) The DAC of claim 27 wherein means for connecting comprises means for connecting each of the plurality of sub DACs with at least one other of the plurality of sub DACs to share charge and generate at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal.

50. (New) The DAC of claim 34 further comprising means for generating at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal in response to the charge stored on each of the plurality of capacitors by the step of charging.

51. (New) The DAC of claim 34 wherein means for connecting comprises means for connecting each of the plurality of sub DACs with at least one other of the plurality of sub DACs to share charge and generate at least one analog signal indicative of a sum of the values of the bits in the multi-bit digital signal.

52. (New) The DAC of claim 37 wherein each of the plurality of sub DACs shares charge with at least one other of the plurality of sub DACs to generate at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

53. (New) The DAC of claim 37 wherein the switched capacitor network generates the at least one analog signal in response to the charge received by the capacitance of each of the plurality of sub DACs in response to the associated bit.

54. (New) The DAC of claim 39 wherein each of the plurality of sub DACs shares charge with at least one other of the plurality of sub DACs to generate at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

Amendments Filed are Coded as Follows:

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8/15/02 = **bold text**
2/13/03 =

55. (New) The DAC of claim 39 wherein the switched capacitor network generates the at least one analog signal in response to the charge received by the capacitance of each of the plurality of sub DACs in response to the associated bit.

56. (New) The DAC of claim 1 wherein the DAC has more than one charge sharing operating state in which at least two of the plurality of sub DACs share charge with one another.

57. (New) The DAC of claim 1 wherein the DAC has more than one operating state, subsequent to the charge sharing operating state, in which the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

58. (New) A DAC comprising:

a switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, the DAC having an operating state in which at least two of the plurality of sub DACs share charge with one another, and having an operating state in which fewer than all of the plurality of sub DACs are connected to an output terminal and the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

59. (New) The DAC of claim 58 wherein the DAC has more than one charge sharing operating state in which at least two of the plurality of sub DACs share charge with one another.

Amendments Filed are Coded as Follows:

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8/15/02 = **bold text**
2/13/03 =

60. (New) The DAC of claim 58 wherein the DAC has more than one operating state in which fewer than all of the plurality of sub DACs are connected to an output terminal and the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

61. (New) The DAC of claim 58 wherein in the operating state in which fewer than all of the plurality of sub DACs are connected to an output terminal and the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal, the sub DACs that are connected to the output terminal deliver charge to said output terminal.

62. (New) A method of converting a multi-bit digital signal to an analog signal indicative of a sum of value of each bit in the multi-bit digital signal comprising the steps of:

charging each of a plurality of capacitors to a value corresponding to a value of a bit in the multi-bit signal, wherein the charge on each capacitor corresponds to a weight of the value of a corresponding bit;

connecting at least two of the plurality of capacitors to one another to share charge; and

connecting fewer than all of the plurality of sub DACs to an output terminal to provide at least one analog output signal indicative of a sum of values of each bit in the multi-bit signal.

Amendments Filed are Coded as Follows:

1/14/02 =

8/15/02 = **bold text**

2/13/03 =

63. (New) A DAC comprising:

means for charging each of a plurality of capacitors to a value corresponding to a value of a bit in a multi-bit signal, wherein the charge on each capacitor corresponds to a weight of the value of a corresponding bit;

means for connecting at least two of the plurality of capacitors to one another to share charge; and

means for connecting fewer than all of the plurality sub DACs to an output terminal to provide at least one analog output signal indicative of a sum of values of each bit in the multi-bit signal.

64. (Amended) An integrated circuit comprising:

an integrated switched capacitor network that receives a multi-bit digital signal, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, wherein the associated amount of charge for each of the plurality of sub DACs is in direct proportion to a weight of the bit, the **~~DAC~~ integrated switched capacitor network** having an operating state in which at least two of the plurality of sub DACs share charge with one another, and having an operating state in which fewer than all of the plurality of sub DACs are connected to an output terminal and the switched capacitor network outputs at least one analog signal indicative of a sum of values of each bit in the multi-bit signal.

65. (New) The DAC of claim 15 wherein the angular offset is substantially ninety degrees.

Exhibit B

Claims in the Issued Patent 6,917,321, Filed 07/12/05, and Claims in the Amendments as Filed on 1/14/02, 8/15/02 and 02/13/03

Application Claim No.	Patent Claim No.	Comments
1	1	same
2	2	same
3	3	same
4	4	same
5	16	found but renumbered
6		no corresponding claim
7	5	found but renumbered
8	6	found but renumbered
9	26	found but renumbered
10		no corresponding claim
11		no corresponding claim
12	20	found but renumbered
13	27	found but renumbered
14		no corresponding claim
15	21	found but renumbered
16	22	found but renumbered
17	29	found but renumbered
18		no corresponding claim
19	31	found but renumbered
20		no corresponding claim
21	35	found but renumbered
22		no corresponding claim
23		no corresponding claim
24	36	found but renumbered
25		no corresponding claim
26		no corresponding claim
27	39	found but renumbered
28		no corresponding claim

Application Claim No.	Patent Claim No.	Comments
29		no corresponding claim
30		no corresponding claim
31	48	found but renumbered
32		no corresponding claim
33		no corresponding claim
34	49	found but renumbered
35		no corresponding claim
36		no corresponding claim
37	52	found but renumbered
38	55	found but renumbered
39	56	found but renumbered
40	57	found but renumbered
41	58	found but renumbered
42	12	found but renumbered
43	13	found but renumbered
44		no corresponding claim
45	34	found but renumbered
46		no corresponding claim
47	34	found but renumbered
48	40	found but renumbered
49		no corresponding claim
50	50	same with renumbered dependent claim
51	51	same with renumbered dependent claim
52	53	found but renumbered
53	54	found but renumbered
54	57	found but renumbered
55	58	found but renumbered
56	60	found but renumbered
57	15	found but renumbered

Application Claim No.	Patent Claim No.	Comments
58	59	found but renumbered
59	60	found but renumbered
60	61	found but renumbered
61	62	found but renumbered
62	63	found but renumbered
63	64	found but renumbered
64	65	found but renumbered
65		no corresponding claim